Dear CEG2, CEG3 Students (from AY16 Poly intake)

Mail below FYI too.
1. If you are keen in RfP, please indicate via the same link by end-Feb.
2. IA is non-compulsory for Poly intakes. From your recommended schedule, AY16 Poly also has no UEM space per se i.e. if you are still keen to register for SIP/VIP, the 6 MCs (CS/CU) will count on top, and above the total (minimum) MCs for graduation.
3. Understand some of you are taking CG3002 in the current semester.

Regards
Winnie

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Dear CEG2 Students

1. Three pathways
As informed earlier, the three pathways takes effects for all Engineering students starting AY16 intake. If you still haven’t, please refer to the pathway mappings for CEG AY2016/17 (PS: linked via FFG Checklists page).
By default, all of you have been tagged to the Practising Professional Pathway (PPP). Students in the Innovation & Design-Centric Programme would have been re-tagged to the corresponding iDCP.
If you are keen in the Research-focused Pathway (RfP), please indicate via this link by 28 Feb.

2. Compulsory IA/internship
ATAP/SIP and IA/VIP are administered at School/Faculty level. Understand from my Sch/Fac colleagues that IA application (for IA in May/June – Nov/Dec 2018 i.e. sem 1, AY2018/19) will be opened to eligible students next Mon (5 Feb). A copy of the eblasts (sent by FoE/SoC administrator) will be uploaded to CEG IA page as and when available.

Please ensure you read through CEG IA page, in particular:
- AY2014/15 intake & after: Students are NOT allowed to take two rounds of 3-months internship, in lieu of 6-months (compulsory) IA. In view of compulsory IA (typically in Year 3), CG3002 and EE3204 will be offered in both semesters ONLY IF a minimum enrolment is met. CG3207 will be offered in semester 1 (only), as an evening module.
- While CEG students may apply for industrial attachment OR internship, via either FoE (IA/VIP) or SoC (ATAP/SIP), please DO NOT apply both sides, then decide on the 'preferred' offer - it does not leave a positive impression to reject an offer. Also, it will affect another applicant.
FYI, a couple of your seniors (unfortunately) did just that and found themselves tied up in knots, due to having to keep up with the different timelines and rules (amidst their modules’ assessments).

3. CG3002 Embedded Systems Design Project in AY2018/19
CG3002 (6 MCs) is a CEG core (project) module/Major requirements that is typically scheduled for Year 3. For whatsoever reason, the bulk of your seniors (from AY14 and AY15 intakes) preferred to take CG3002 in sem 1 (Year 3), then go for IA in sem 2 (Year 3), causing a lopsided enrolment for CG3002.

However, due to a bigger enrolment for CEG AY16 intake and (lab) space constraints, it would Not be possible to accommodate all of you (for CG3002 lab) in a single semester. Hence, this serves to pre-empt that in AY2018/19*, CG3002 will be/has to be offered in both semesters, with a cap on enrolment of 90 students per semester. Your seniors had been able to secure CG3002 with 1 bid point. While we hope that can continue for AY16 intake, it can only happen if some of you (in PPI) heed the advisory and apply for IA next week (during ATAP/IA application round 1) i.e. go for IA in sem 1, AY18/19, then take CG3002 in sem 2, AY18/19.

Students in RfP are encouraged to take CS3209 CS Research Methodology OR EG2605 UROP (as UEM) in sem 1, AY18/19, then CG3002 in sem 2, AY18/19 (then SIP/VIP in May - Aug 2019).

*Due to curriculum changes for AY2017/18 intakes, CG3002 will cease to be offered in AY2019/20 as it will be replaced by CG4002 (8 MCs).
Affected students (e.g. who went for SEP or NOC year-long programmes) will have to read CG4002 (in lieu of CG3002). If you have already secured a SEP placement (for exchange in AY18/19), please re-look your study plan to accommodate FYP (CG4001) with CG4002 (in lieu of CG3002) in your final year (preferably without delaying graduation).

Let us know if you have any queries.

Regards
Winnie

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